REMARKS

The Examiner is thanked for the careful review of this Application. Claims 6-8 and 26-35 are pending after entry of the present Amendment. Claims 27 and 33 were amended to correct typographical errors. Claims 1-5 and 9-25 were cancelled. This Amendment is being presented in the new format, as suggested.

Objections to Claims:

Per Office's request, Applicants have amended claims 27 and 33 to correct lack of antecedent basis as pointed out by the Office. Accordingly, Applicants respectfully request that objections to the claims be withdrawn.

Rejections under 35 U.S.C. § 103(a):

Applicants respectfully request reconsideration of rejection of claims 6-8 and 26-35 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,333,255 to Sekiguchi in view of U.S. Patent No. 6,277,728 to Ahn et al. (hereinafter referred to as "Ahn"). As will be explained below, the combination of Sekiguchi and Ahn does not raise a *prima facie* case of obviousness against the subject matter defined in independent claims 6, 28, and 34. First, this combination does not teach or suggest all of the features defined in independent claims 1, 28, and 34. Second, the necessary suggestion or motivation to combine the references in the manner proposed by the Office is missing.

Considering first whether the combination teaches or suggests all of the claimed features, it is respectfully submitted that the multilevel structures implementing gas-dielectric as shown in Sekiguchi in view of the multilevel interconnect structure having an outer low-K dielectric coating as shown in Ahn fails to teach or suggest all of the features of the claimed invention, as defined in independent claims 6, 28, and 34.

Specifically, Sekiguchi teaches forming a plurality of MOS transistors each including source/drain regions, sidewalls, a gate oxide film, a gate electrode, a gate wire on a substrate, a substrate coating that covers the gate electrodes and wires. Each structure level includes a lower and upper SiO_2 films being used as stoppers and insulators. Lower and upper carbon films are also used as provisional films with plugs being formed in the lower carbon films and

the trenches for wiring being formed in the upper carbon film. A layer of barrier film and a Copper layer are sputtered over the surface of the substrate filling the trenches and the contact holes. A dummy opening is made through all the carbon layers, SiO_2 layers, and the substrate coating. The carbon films are then removed by ashing leaving the gas layers formed between the barrier metal film and the copper alloy film as well as the lower and upper SiO_2 films. In this structure, the interconnection between the wires and the plugs is enhanced by the upper and lower SiO_2 films which the lower and upper SiO_2 films laterally interconnect the wires of each layer to each other.

Citing to Sekiguchi, the Office asserts that the two inside lines having reference number 17 are the supporting stubs of the claimed invention. The Office further contends that it is inherent that the two inside lines provide support for the structure. Applicants respectfully submit that contrary to the Office' assertion, the two inside "lines" shown in Sekiguchi are just wires used to provide connection between the multiple levels of the semiconductor structure. The Figures provided in Sekiguchi are exemplary cross-sectional views of the semiconductor device taught in Sekiguchi. As such, viewing a different cross section of the semiconductor device would depict the clear definition of the trenches and contacts which together constitute the wires depicted in the middle of the structures shown in Sekiguchi.

As shown in Figures 1(a)-9, each of the two inside lines are defined within the carbon film 10a and over the substrate coating such that each inside line is in contact with a source/drain region 3. That is, each of the alleged supporting columns, the inside lines, is constructed from a plurality of contacts and trenches are configured to provide electrical connections within the structure. Each contact or trench is lined with the barrier metal film and is filled with the copper alloy.

The next reference, Ahn et al. defines a multilevel interconnect structure that includes an outer low-K dielectric coating. Ahn deposits a layer of photoresist on a substrate assembly, etches the photoresist to form openings, deposits a metal layer on the photoresist layer so as to fill the openings, and remove the photoresists. At this point, an upper level conductive metal layer that is supported by the metal filling the openings is formed on the photoresist. The upper level of the interconnect structure is coated with a low-k dielectric film which is subsequently planarized.

As can be appreciated, Ahn fails to teach or suggest using a plurality of supporting stubs that are configured to form supporting columns. Rather, Ahn teaches that the metallization lines are supported by the lower level metal layers. As such, Ahn does not need to use any additional stubs to support the metallization lines, as according to Ahn adequate support is provided without the stubs. Thus, Ahn does not teach or suggest using the supporting stubs.

Additionally, although the carbon films (i.e., the dielectric layers) shown in Sekiguchi are ashed and removed, the SiO_2 layers remain intact in the multilevel structure of Sekiguchi. Thus, as explicitly taught by Sekiguchi, the SiO_2, layers provide the structural integrity for the multilevel semiconductor device and so long as the SiO_2 layers are present, the integrity of the structure is maintained. Accordingly, neither Sekiguchi nor Ahn teach or suggest a semiconductor structure that includes a substrate having a plurality of transistor devices and a plurality of copper interconnect metallization lines and conductive vias that are isolated from each other by a porous dielectric material. Rather, in one example, Sekiguchi replaces the carbon layers with low-K dielectrics. But, even in that embodiment, the SiO_2 layers remain intact. That is, Sekiguchi uses the low-K dielectric material so as to provide additional support to the wires which integrity is being maintained by the SiO_2 layers. Specifically, none of the embodiments depicted in Sekiguchi teach or suggest not including the SiO_2 or what can one expect in such a case.

In a like manner, Ahn fails to teach or suggest using porous dielectric material to isolate the metallization lines and vias. As such, the combination of Sekiguchi and Ahn fails to teach or suggest using the porous dielectric material without the SiO_2 layers, to maintain the integrity of the semiconductor device, as defined in the claimed invention. Furthermore, neither Sekiguchi nor Ahn teach or suggest adding a passivation layer to the semiconductor device, as defined in claim 34.

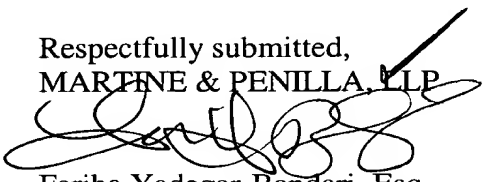
Moreover, a primary function of Ahn is to reduce the number of dielectric deposition cycles. As such, Ahn and Sekiguchi are not combinable so that the objective of Ahn and S can both be achieved. One reading Ahn would be discouraged from using the lower and upper carbon layers and SiO_2 layers taught in Sekiguchi, and without these features, the semiconductor device of Sekiguchi cannot provide sufficient

integrity to support the multilevel structure. Furthermore, as described in more detail above, even if Sekiguchi and Ahn were combinable, the resulting semiconductor structure does neither include the supporting stubs of the claimed invention nor does the combination supports implementing a porous dielectric material in the semiconductor device.

Accordingly, for at least the above-stated reasons, independent claims 6, 28, and 34, are patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn. Claims 7, 8, 26, and 27, 29-32, and 35, each of which ultimately depends from the applicable independent claim 6, 28, and 34 are likewise patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn for at least the same reasons set forth for the applicable independent claim.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6913. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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